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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,174	02/15/2001	Kenneth C. Yeager	062986.0174	4017

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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,174	YEAGER ET AL.	
	Examiner	Art Unit	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claims 1-20 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 6-15 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 6,618,775 of Davis in further view of US Patent No. 5,491,793 of Somasundaram et al. referred hereinafter "Somasundaram".

In regards to claim 1, Davis discloses an integrated circuit comprising:

a central processing unit (see column 3 lines 44-47);

a trace recorder operable to capture selective information passed from the central processing unit to the memory immediately prior to and immediately subsequent to a triggering event (see column 8 lines 30-35), the trace recorder including a memory array(see figure 9 item 910 and figure 10), the trace recorder operable to continuously capture selective information in a selective first set of blocks of the memory array prior to the triggering event, the trace recorder operable to capture information subsequent to the triggering event in a second set of blocks of the memory array without writing over information captured prior to the triggering event in the first set of blocks of the memory array (see column 8 lines 5-40).

However, Davis fails to disclose:

an instruction cache in communication with the central processing unit;

a data cache in communication with the central processing unit;

Somasundaram discloses "to reduce access time of instruction/data, CPU employs an hierarchical memory architecture. Under such memory architecture, instruction and data from the

external memory are first staged respectively into an 32-bit wide instruction cache and a 32-bit wide data cache" (see column 4 lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the memory to include an instruction cache in communication with the central processing unit and a data cache in communication with the central processing unit, such that a trace recorder operable to capture selective information passed from the central processing unit to the instruction and data cache. A person of ordinary skill in the art would have been motivated because Davis discloses using memory, and instruction and data cache constitute as memory that is well known to reduce access time of accessing instructions and data, as per teaching of Somasundaram (see column 4 lines 45-50).

In regards to claim 6, Davis discloses wherein the trace recorder is operable to inhibit capturing of information (see figure 9 items 912, 944 and column 7 lines 20-67).

In regards to claim 7, Davis discloses wherein the trace recorder is operable to provide captured information to a device external to the integrated circuit (see column 3 lines 48-49).

In regards to claim 8, Davis discloses wherein the trace recorder is operable to store captured data in non-consecutive storage locations (see column 4 lines 5-20).

In regards to claim 9, Davis discloses wherein the trace recorder is operable to capture data every Nth operating cycle (see column 7 lines 40-45 and column 8 lines 5-20)

In regards to claim 10, Davis discloses wherein the trace recorder is operable to maintain captured information associated with the first and second triggering event despite the occurrence of a third trigger event (see column 4 lines 10-15, 35-50 and column 8 lines 30-35).

In regards to claim 11, Davis discloses a method of recording trace data in a microprocessor based integrated circuit, comprising:

identifying a triggering event (see column 3 lines 44-47);

capturing information transferred from a central processing unit to a memory (see figure 4 and column 3 lines 44-47)

wherein the information is captured immediately prior to and immediately subsequent to the triggering event (see column 8 lines 30-35), wherein the information is continuously captured in a selective first set of blocks of a memory array prior to the triggering event, wherein the information is captured subsequent to the triggering event in a second set of blocks of the

memory array without writing over information captured prior to the triggering event in the first set of blocks of the memory array (see column 8 lines 5-40).

However, Davis fails to disclose

capturing information transferred from a central processing unit to an associated instruction cache pertaining to the triggering event;

capturing information transferred from a central processing unit to a data cache pertaining to the triggering event.

Somasundaram discloses "to reduce access time of instruction/data, CPU employs an hierarchical memory architecture. Under such memory architecture, instruction and data from the external memory are first staged respectively into an 32-bit wide instruction cache and a 32-bit wide data cache" (see column 4 lines 45-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the memory to include an instruction cache and a data cache, such that recording trace data comprises capturing information transferred from a central processing unit to an associated instruction cache pertaining to the triggering event and capturing information transferred from a central processing unit to a data cache pertaining to the triggering event. A person of ordinary skill in the art would have been motivated because Davis discloses using memory, and instruction and data cache constitute as memory that is well known to reduce access time of accessing instructions and data, as per teaching of Somasundaram (see column 4 lines 45-50).

In regards to claim 12, Davis discloses wherein information pertaining to the triggering event is captured and maintained despite the occurrence of a subsequent triggering event (see column 4 lines 10-15, 35-50 and column 8 lines 30-35).

In regards to claim 13, Davis discloses wherein information is captured in non-consecutive storage locations (see column 4 lines 5-20).

In regards to claim 14, Davis discloses outputting captured information (see column 3 lines 48-49).

In regards to claim 15, Davis discloses wherein information is captured for every Nth cycle associated with the operation of the central processing unit (see column 7 lines 40-45 and column 8 lines 5-20).

Claims 2-5 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Davis in view of Somasundaram and in further view of US Patent No. 5,886,998 of Voith et al. referred hereinafter "Voith".

In regards to claim 2, Davis discloses wherein the trace recorder operable to capture information associated with both a first triggering event and a second triggering event (see column 4 lines 5-15).

Davis further discloses the trace recorder as circular buffers (see column 4 lines 5-15). Davis, however, fails to explicitly teach wherein the trace recorder is a single memory unit.

Voith discloses circular buffers as a single memory unit, indicating the trace recorder is a single memory unit (see figure 12 and column 10 lines 8-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention wherein the trace recorder is a single memory unit. One of ordinary skill in the art at the time of the invention would have been motivated because Davis discloses the trace recorder as circular buffers, and Voith teaches circulars buffers as a single memory unit (see figure 12 and column 10 lines 8-15).

In regards to claim 3, Davis discloses wherein the trace recorder is operable to maintain captured information prior to and associated with the first triggering event upon occurrence of the second triggering event (see column 4 lines 10-15, 35-50 and column 8 lines 30-35).

In regards to claim 4, Davis discloses wherein the trace recorder is operable to capture information subsequent to and associated with the first triggering event upon the occurrence of the second triggering event (see column 4 lines 10-15, 35-50 and column 8 lines 30-35).

In regards to claim 5, Davis discloses wherein the trace recorder is operable to capture information associated with the second triggering event prior to and subsequent to the second triggering event (see column 8 lines 30-35).

Claims 16-20 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Davis in further view of Somasundaram and Microsoft computer dictionary 3rd ed. referred hereinafter "Microsoft".

In regards to claim 16, Davis discloses a trace recorder for a microprocessor based integrated circuit, comprising:

a memory array operable to capture information passed from a central processing unit to a memory of the integrated circuit (see figure 9 item 910 and figure 10);

a trigger control register operable to initiate information capture (see figure 7 item 750);

a capture control register operable to determine how information is to be captured and maintained (see figure 7 item 770);

wherein the information is captured immediately prior to and immediately subsequent to the triggering event (see column 8 lines 30-35), the memory array operable to continuously capture selectively information in a selective first set of blocks of the memory array prior to the triggering event, the memory array operable to capture information subsequent to the triggering event in a second set of blocks of the memory array without writing over information captured prior to the triggering event in the first set of blocks of the memory array (see column 8 lines 5-40).

Davis further discloses the use of address counter, which is used to determine where information is to be captured within the memory array (see column 7 lines 39-45).

However, Davis fails to explicitly disclose:

an order map register operable to determine where information is to be captured within the memory array

to capture information passed from a central processing unit to instruction and data caches of the integrated circuit

Microsoft discloses a register as a high-speed memory used to hold data for a particular purpose (see page 402 search term "register").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a register with the address counter. A person of ordinary skill in the art would have been motivated because Davis discloses generating address for the lowest RAM address to the high RAM address (see column 7 lines 40-42), and having a register would provide a means to store the current RAM address, thus enabling determining where information is to be captured within the memory address. Furthermore, Davis discloses when a trigger

occurs, data is read out form the oldest data to the newest data (see column 8 lines 5-25). A register storing the current value would provide a reference to the oldest data.

Furthermore, Somasundaram disclose "to reduce access time of instruction/data, CPU employs an hierarchical memory architecture. Under such memory architecture, instruction and data from the external memory are first staged respectively into an 32-bit wide instruction cache and a 32-bit wide data cache" (see column 4 lines 45-50)

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the memory to include an instruction cache and a data cache, such that information is captured from the central processing unit to instruction and data caches of the integrated circuit. A person of ordinary skill in the art would have been motivated because Davis discloses using memory, and instruction and data cache constitute as memory that is well known to reduce access time of accessing instructions and data, as per teaching of Somasundaram (see column 4 lines 45-50).

In regards to claim 17, Davis discloses an inhibit mask register operable to selectively inhibit capturing of information (see column 5 lines 63-67).

In regards to claim 18, Davis discloses control logic operable to access the memory array according to the trigger control register, the capture control register, and the order map register. (see figure 9 items 920, 960 and 930 and column 7 lines 10-67).

In regards to claim 19, Davis discloses control logic generates memory addresses to the memory array (see figure 9 items 920, 960 and 930 and column 7 lines 10-67).

In regards to claim 20, Davis discloses wherein information associated with the triggering event is maintained in the memory array during capture of information associated with a subsequent triggering event (see column 4 lines 10-15, 35-50 and column 8 lines 30-35).

Response to Arguments

Applicant's arguments filed January 19, 2005 have been fully considered but they are not deemed to be persuasive.

In response to applicant's argument "As a result, the Davis patent fails disclose the use of first and second sets of blocks in a memory for respectively capturing information prior to and subsequent to a triggering event and also fails to disclose an ability to capture information subsequent to the triggering event without writing over previously captured information prior to the triggering event as provided in the claimed invention" (see bottom paragraph page 8), examiner respectfully disagrees.

Davis discloses the circular buffer could be configured so that trace data is selectively captured before, after, or around the occurrence of the triggering event"(see column 8 lines 30-35), thus clearly teaching capture information immediately prior to and immediately subsequent to a triggering event. The blocks used to capture data prior to a triggering event constitute a first set of blocks and blocks used to capture data subsequent to a triggering event constitute a second set of blocks. Furthermore, during the first instance that information is written to the blocks, there is no writing over information since there is no information in the blocks. Examiner maintains his rejection.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ecp
3/17/05

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